

USING GENETIC ALGORITHM TO OPTIMIZE THE DESIGN OF CHARGE PUMP CIRCUITS

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Received 17.09.2024.
Revised 14.11.2024.
Accepted 21.12.2024.

Keywords:

Integrated CP design, Dickson CP, Cockcroft-Walton CP, Genetic algorithm.

Original research



ABSTRACT

Charge pump power converters in integrated form are used to produce different d.c. levels. The output voltage, voltage ripple, and required chip area (total capacitance) are some of the most significant performance factors that could have an impact on circuit operation. A trade-off between the aforementioned factors is necessary to improve these parameters. In this study, genetic algorithm (GA) is used as an optimization technique to produce the best design that meets predetermined criteria. The genetic algorithm is used to minimization the chip area (total capacitance) by increasing the number of stages. It is established Constraining factors also include other performance metrics. The obtained parameter values preserve performance while meeting the fitness function's minimal requirements, which include the needed chip area (total capacitance).

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1. INTRODUCTION

A charge pump circuit is an electrical circuit that converts the source voltage VDD into a much higher DC output voltage. Charge pumping circuits (CPs) consist solely of switches and capacitors, as opposed to other conventional DC-DC converters that also use inductors. (Dickson, 1976; Palumbo et al., 2002). Capacitors are used as storage components in charge pump circuits, whereas transistors and diodes serve as transfer switches. The drain and source terminals are the two switch terminals, whereas the gate terminal controls the switch gate. Various applications, including smart power and non-volatile memory like flash or EEPROM, to write or erase floating-gate devices (Jinbo et al., 1992; Palumbo et al.,

2006; Palumbo & Pappalardo, 2010; Umezawa et al., 1992), operational amplifiers, voltage regulators, switching capacitor circuits, SRAMS, and LCD drivers (Ying et al., 2003) are most important applications of CPs. Charge pump circuits are realized in many different structures. The most important topologies may include Dickson and Cock-croft-Walton (Tanzawa & Tanaka, 1997; Cockcroft & Walton, 1932) This work introduces a genetic algorithm-based optimization strategy for two charge pump topologies: Cockcroft-Walton and Dickson CP. The most important of them is the Dickson charge pumps are rather common since they may be used on the same host system and the voltage gain of these two topologies is proportional to the stages number the pump uses. These topologies of a charge pump are investigated

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to find how load current affected output voltage for non-volatile memory application. The voltage of output without load effect where it is expressed (Dickson, 1976; Matoušek et al., 2017):

$$V_o = (V_{in} - V_d) \cdot (N + 1) \quad (1)$$

Where V_{in} is the input voltage, V_o is the output voltage without a load, V_d is the voltage drop, and N is the number of stages.

Output voltage when load is applied :

$$V_{out} = V_o - R_{out} \cdot I_{out} \quad (2)$$

where V_{out} is the output voltage at load, V_o is the output voltage when no load is applied, and R_{out} is the output resistance.

Define the output resistance for Dickson charge pump as (Palumbo et al., 2000):

$$R_{out} = \frac{N}{f \cdot C} \quad (3)$$

and Cockcroft-Walton charge pump as (Pulvirenti, 2022):

$$R_{out} = \frac{1}{f \cdot C} 2 \sum_{i=1}^{\frac{N}{2}} i^2 \quad N \text{ even} \quad (4)$$

$$R_{out} = \frac{1}{f \cdot C} \cdot \left[\sum_{i=1}^{\frac{N+1}{2}} i^2 + \sum_{i=1}^{\frac{N-1}{2}} i^2 \right] \quad N \text{ odd} \quad (5)$$

Where R_{out} denotes the output resistance, f the clock frequency, C the pumping capacitance, and N the number of stages. Since the capacitance value is related to chip size, the goal of the genetic algorithm is to minimize the size of the pumping capacitance for two topologies of charge pumps. The pumping capacitance is minimize at the expense of increasing the number of stages while maintaining the required performance and specifications (Asif et al., 2020).

2. CHARGE PUMP TOPOLOGIES

The Dickson-Cockcroft-Walton charge pump shown in Figure 1 and Figure 2 consists of charge transfer diodes and charge pumping capacitors. The control of the charging and discharging mechanisms in the pumping capacitors is based on non-overlapping clock pulses (Navidi, 2018). To increase the output voltage, the circuit gradually pumps charge from the power source to the output terminal. Due to the presence of the threshold voltage of the diode, which acts as a switch for transferring charge to the output, there will be a drop in

the output voltage. The Dickson charge pump circuit was introduced as an improvement over the Cockcroft-Walton charge pump. Since the capacitors in the Cockcroft-Walton CP are connected in series, it turns out to have a high output resistance, which means that as the number of stages increases, the output resistance increases. The Cockcroft-Walton CP circuit is not recommended for use in integrated circuits because it only allows efficient multiplication if the coupling capacitors are much larger than the capacitance of the stray circuit (Peng, 2020). The capacitors in the Dickson charge pump are connected in parallel and must be robust enough to withstand the full output voltage.

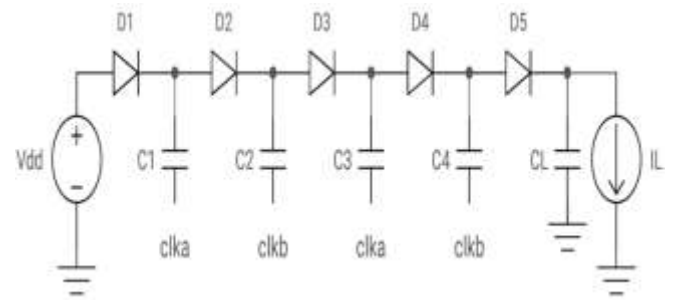


Figure 1. Four stage Dickson CP

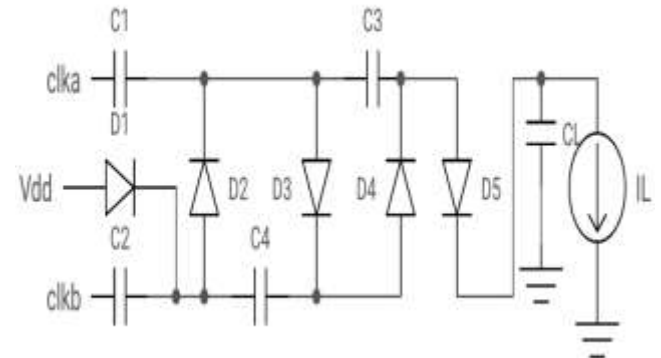


Figure 2. Four stage Cockcroft-Walton CP

The disadvantage of these circuits is the voltage drop that occurs due to the use of diodes (Anil & Sharma, 2012). As a result, as with the number of stages, so with the output resistance.

3. GENETIC ALGORITHM APPLICATION

Genetic algorithms combine the notion of natural selection or "survival of the fittest" with other evolutionary processes to generate continuous iterations, known as generations, of solutions that are superior to the previous one (Pohlheim, 2004). The optimization method aims to either maximize or minimize a parameter or combination of parameters (Baker, 1998). Whereas minimizing a function, for example $f(x)$, while maximizing is the inverse, $-f(x)$, this paper, almost a minimization problem. Dickson and Cockcroft-Walton

use this for designing and implementing standard charge pump circuits, where it is found that the pumping capacitor of the Cockcroft-Walton CP is larger than the pumping capacitor of the Dickson CP because the Cockcroft-Walton charge pump suffers from a high output resistance (Pulvirenti, 2022). Determining the design's topology is the first stage in the GA process. The main duties associated with minimization operations are to establish the parameters, restrictions, and search variables in a suitable way. The number of stages (N) and the clock frequency (f) and output voltage (Vout) are intended to be the variables, and all necessary requirements and constraints such as the ripple voltage (Vr).

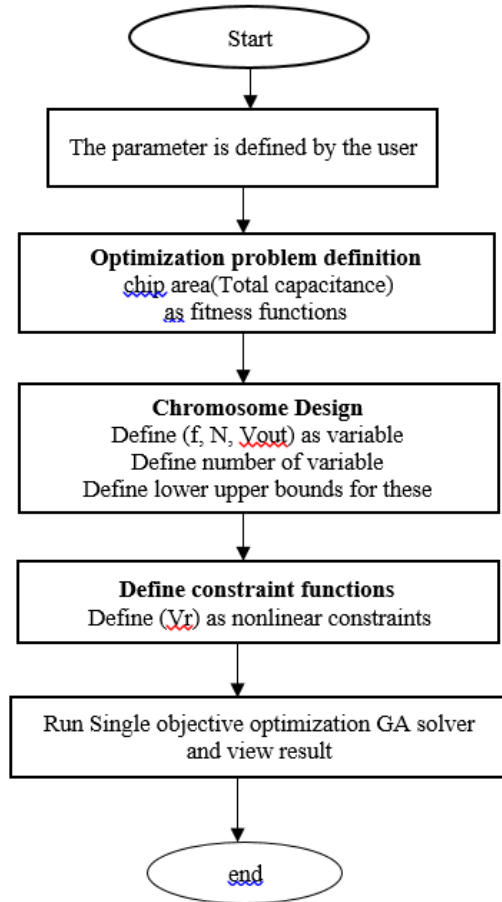


Figure 3. Flowchart of Genetic algorithm procedure based on MATLAB

The optimization toolbox approach in MATLAB is used to implement the genetic algorithm processes and this process can be illustrated in general as in the Figure 3.

4. OPTIMIZATION FOR CHIP AREA (TOTAL CAPACITANCE) FOR DICKSON AND COCKCROFT-WALTON CHARGE PUMP

In this paper, a genetic algorithm was used to improve the chip area (total capacitance) to apply non-volatile memory by minimizing the value of the total capacitance

depending on increase the number of stages. The fitness functions are given as single-objective functions. The genetic algorithm will be terminated if the number of generations reaches 500. Expressing the function of fitness in general as (Mitchell, 1998):

$$Fitness(x) = Fit(x) \quad (6)$$

5. PERFORMANCES EVALUATION

The minimization of the chip area (total capacitor) using genetic algorithm affects the other performance of CP circuits. The design equations for the Dickson and Cockcroft-Walton configurations can be derived, which include the pumping capacitance and the ripple voltage. The pumping capacitance of the Dickson charge pump may be represented as the following (Palumbo et al., 2002):

$$C_p = \left[\frac{N}{(N+1)V_{dd} - V_{out}} \right] \cdot \frac{IL}{f} \quad (7)$$

The pumping capacitance of the Cockcroft-Walton CP is also expressed in terms of the number of stages, whether the stages are even or odd, and is expressed as (Ismail, 2015):

$$C_p = \left[\frac{N(N+1)(N+2)}{(N+1)V_{dd} - V_{out}} \right] \cdot \frac{IL}{12 \cdot f} \quad N \text{ odd} \quad (8)$$

$$C_p = \left[\frac{(N+1)(N^2 + 2N + 3)}{(N+1)V_{dd} - V_{out}} \right] \cdot \frac{IL}{12 \cdot f} \quad N \text{ even} \quad (9)$$

where f denotes the clock frequency, N the number of stages, Vdd the power supply, Vout the output voltage, and IL the load current.

Ripple voltage was expressed as (Shen, 2015):

$$V_r = \frac{IL}{f \cdot CL} \quad (10)$$

6. COMPARISON BETWEEN GA AND MATHEMATICAL RESULTS

The genetic algorithm routine in this paper is used to focus on minimizing the chip area (total capacitance) at the expense of increasing the number of stages for a non-volatile memory application (Kawahara et al., 1996; Sawada et al., 1995) where the load current (IL = 50uA) and the load capacitance (CL = 10pF) are used, where the chip area (total capacitance) optimization is used for different number of stages, the pumping capacitor is considered as a fitness function and the supply voltage is 5V, initially, the clock frequency is considered fixed and its value is 10MHz and the output voltage is considered as the target that can be reached (Vout = 25V). Tables 1 and table 2 show a comparison between the results of the genetic algorithm and its mathematical counterpart for two models for the number of stages, where the genetic

algorithm for these values improves the necessary fitness variables significantly and it can be seen that the optimization leads to a significant improvement in minimizing the chip area (total capacitance) compared to the mathematical results. Tables 3 and table 4 also show the optimization process for Cockcroft-Walton and Dickson charge pumps by minimizing the chip area (total capacitance) based on increasing the number of stages at 10MHz frequency. It is observed that the pumping capacitor of Cockcroft-Walton charge pump is large as this pump suffers from output resistance and the total capacitance is given by(Liu, 2012). Hence the frequency is considered variable (10MHz-150MHz) and the ripple voltage is taken as a constraint. Tables 5 and 6 show the improvement of charge pumps by minimizing the chip area (total capacitance) depending on increasing the number of stages with change in frequency and the total capacitance can be expressed as follows:

$$C_{total} = N \cdot C_p \quad (11)$$

Table 1. Comparison between GA results and mathematical results for Dickson CP

Specification	Mathematical results	GA results
Clock frequency	10MHz	10MHz
Number of stages	N = 4	N=17
Output voltage(V)	24.9	25
Total capacitance C	0.4uF	22.1pF
Ripple voltage(V)	0.5	0.5

Table 2 .Comparison between GA results and mathematical results for Cockcroft-Walton CP

Specification	Mathematical results	GA results
Clock frequency	10MHz	10MHz
Number of stages	N = 4	N=17
Output voltage(V)	24.9	25
Total capacitance C	0.4uF	639.5pF
Ripple voltage(V)	0.5	0.5

7. SIMULATION RESULTS

To verify the CP circuit generated by the parameter values provided by GA. Advanced Design System (ADS) is used to simulate the CP circuits under load current $I_L = 50\mu A$ and load capacitor $C_L = 10pF$ for non-volatile memory implementation like EEPROM using 10MHz clock frequency. Both the circuits are designed by Dickson and Cockcroft-Walton using ideal diode in Advanced Design System(ADS). These circuits are also designed and simulated simultaneously for the results given by genetic algorithm like pump capacitance and supply voltage. The transient responses resulting from the comparison of two types of stages are shown in Figure 4 and Figure 5. Table 3 and table 4 also show the comparison between the genetic algorithm results and the simulation results for the output voltage as well as the mathematical results and simulation results for the output resistance of Dickson, Cockcroft-Walton charge pump in

terms of increasing number of stages. The transient responses of these designs are shown in Figure 6 and Figure 7 for the output voltage and output resistance resulting at 10MHz. The work is also illustrated in Table 5 and 6 for comparing the genetic algorithm results and simulation results for the output voltage as well as the mathematical results and simulation results for the output resistance of the Dickson-Cockcroft-Walton charge pump at variable frequency. The transient responses are also shown in Figure 8 and Figure 9 for different types of stages in terms of changing the clock frequency. It is observed that with increasing the number of stages of the charge pump, the output resistance of these designs increases (Pan & Samaddar, 2006). That is, with changing the number of stages, the total capacitance changes at load current $I_L = 50\mu A$, load capacitance $C_L = 10pF$, and supply voltage $V_{dd} = 5V$. An example of the number of stages ($N = 6$) for the Dickson-Cockcroft-Walton topology is also taken as an idea to illustrate the work. Figure 10 and figure 11 shows a five-stage Dickson-Cockcroft-Walton charge pump. The ripple voltage generated by these circuits is inversely proportional to the clock frequency. As the clock frequency increases, the ripple voltage decreases. Table 7 shows the comparison between this work and previous works (Younis et al., 2015).

Table 3. Optimization chip area (total capacitance) and comparison of the results obtained for the Dickson CP at 10MHz

Number of stages	Total Capacitance	Rout Mathematical	Rout Simulation	Vout GA	Vout Simulation
6	18pF	200K Ω	243K Ω	25V	23.6V
8	16pF	400K Ω	486K Ω	25V	23.3V
10	16.6pF	602K Ω	635K Ω	25V	22.8V
13	18.77pF	900K Ω	903K Ω	25V	21V
15	20.4pF	1.1M Ω	1.2M Ω	25V	20.1V

Table 4. Optimization chip area (total capacitance) and comparison of the results obtained for the Cockcroft-Walton CP at 10MHz

Number of stages	Total Capacitance	Rout Mathematica I	Rout Simulation	Vout GA	Vout Simulation
6	84 pF	200K Ω	218K Ω	25V	23.8V
8	120 pF	400K Ω	398K Ω	25V	23.4V
10	183.2 pF	600K Ω	586K Ω	25V	22.53V
13	325 pF	924K Ω	892K Ω	25V	21V
15	465 pF	1.1M Ω	1.04M Ω	25V	20.2V

Table 5. Optimization chip area (total capacitance) and comparison of the results obtained for the Dickson CP at variable frequency

Clock frequency	Number of stages	Total capacitance GA	Vout GA	Vout Simulation	Rout Mathematica	Rout Simulation
16MHz	7	10.22pF	25V	23.6V	300 K Ω	447 K Ω
25MHz	8	6.4pF	25V	23.4V	400 K Ω	340 K Ω
50MHz	10	3.3pF	25V	23.2V	606 K Ω	622 K Ω
100MHz	14	1.96pF	25V	22.2V	1M Ω	1.07M Ω

Table 6. Optimization chip area (total capacitance) and comparison of the results obtained for the Cockcroft-Walton CP at variable frequency

Clock frequency	Number of stages	Total capacitance GA	Vout GA	Vout Simulation	Rout Mathematical	Rout Simulation
16MHz	7	64.4pF	25V	23.5V	298 K Ω	301 K Ω
25MHz	8	48pF	25V	23.4V	400 K Ω	452 K Ω
50MHz	10	36pF	25V	23V	611 K Ω	631 K Ω
100MHz	14	39.2pF	25V	22V	1M Ω	978 K Ω

Table 7. Comparison of the results of this work with the results of other works

Parameter	This work	Previous works
Clock frequency(MHz)	10	10
Supply voltage(V)	5	1.8
Number of stage	17	4
Current load(uA)	50	600
Load capacitance(pF)	10	200
Pumping capacitor(pF)	1.3	66.6
Output voltage (V)	25	5.55

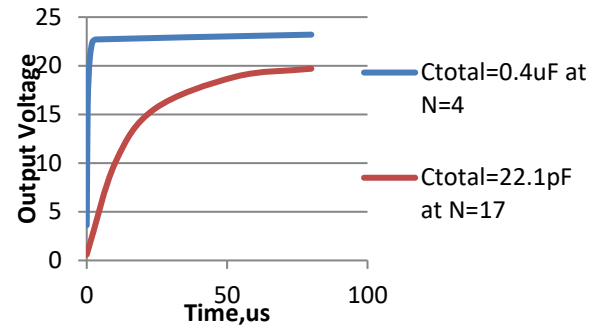


Figure 4. Transient response for Dickson CP for two types of stages

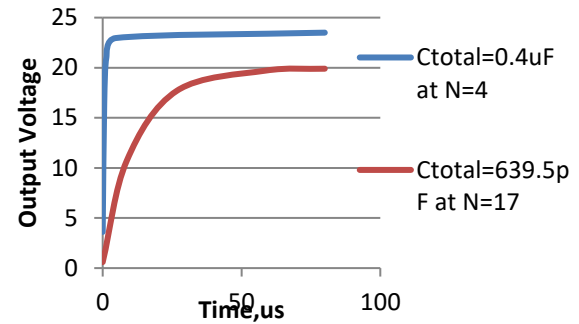


Figure 5. Transient response for Cockcroft-Walton CP for two types of stages

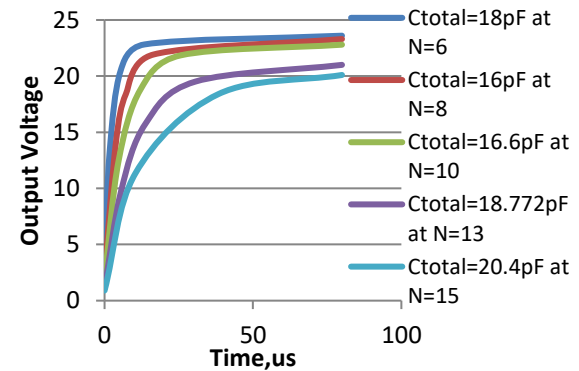


Figure 6. Transient response for Dickson CP for different types of stages at 10MHz

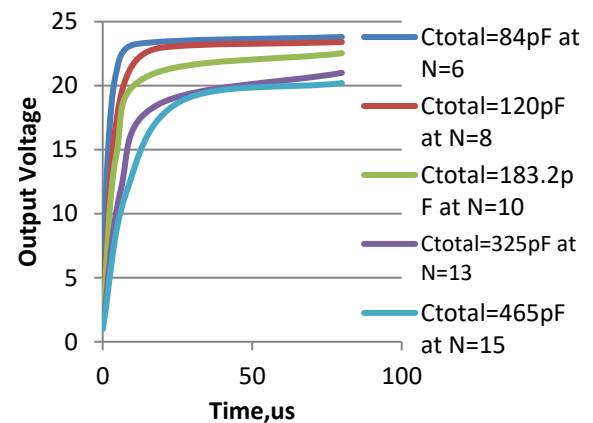


Figure 7. Transient response for Cockcroft-Walton CP for different types of stages at 10MHz

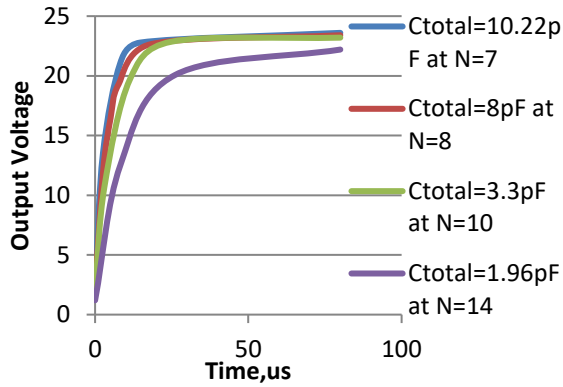


Figure 8. Transient response for Dickson CP for different types of stages at variable frequency

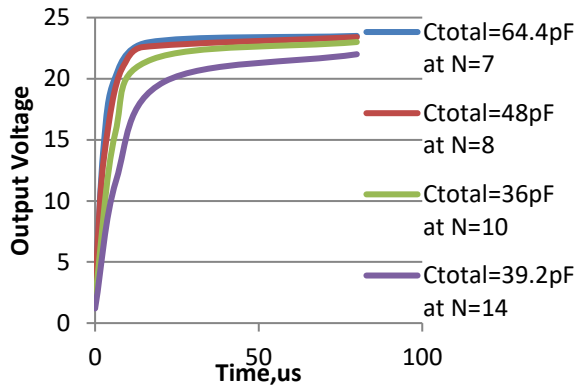


Figure 9. Transient response for Cockcroft-Walton CP for different types of stages at variable frequency

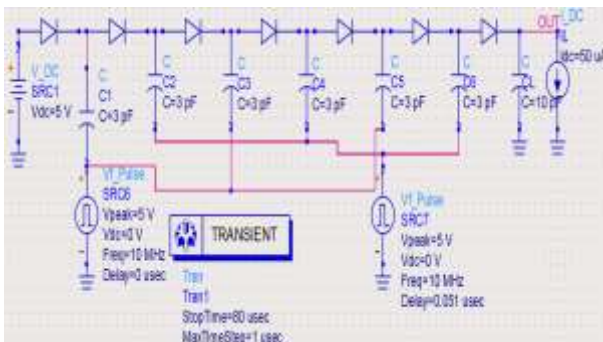


Figure 10. Six stage for Dickson charge pump

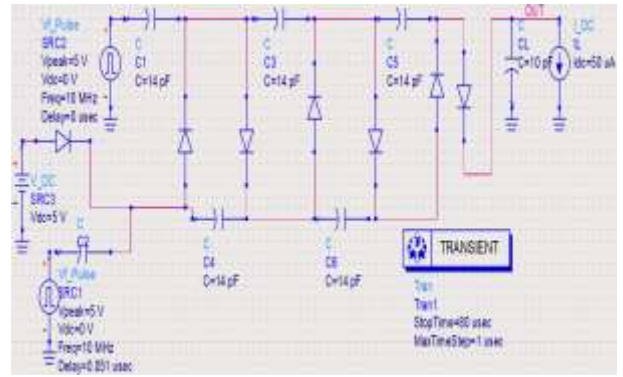


Figure 11. Six stage for Cockcroft-Walton charge pump

8. CONCLUSIONS

The Dickson and Cockcroft-Walton integrated charge pump circuits were investigated in this study's, the circuits performance is improved using genetic algorithms as minimization routine. Minimization for the chip area (total capacitance) depend to an increase in the number of stages. It has been observed that the total capacitance of the Dickson charge pump is less than the total capacitance of the Cockcroft -Walton charge pump because the Cockcroft -Walton charge pump suffers from high output resistance. Utilizing the values of the parameters resulted from the genetic algorithm, simulations of these CP topologies produced suitable outcomes. Subsequently, a comparison was done between these observed results and the mathematical results. An Advanced Design System(ADS) simulation were performed to verify the genetic algorithm results that maintain the required specifications.

Acknowledgement:

The authors of this work are thankful to the University of Nineveh and the College of Electronics Engineering for the support in completing this work.

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